CLAIMS

What is claimed is:

1. A decoupling capacitor for a semiconductor device, said capacitor comprising:

a first low dielectric insulator layer;

a low resistance conductor formed into at least two interdigitized patterns on a surface of the first low dielectric insulator layer, each of said two interdigitized patterns being adjacent the other such that their sidewalls form plates of said capacitor; and

a high dielectric material provided between said two interdigitized patterns.

2. The decoupling capacitor of claim 1, wherein said high dielectric material comprises tantalum pentoxide.

3. The decoupling capacitor of claim 1, wherein said high dielectric material comprises silicon nitride.

4. The decoupling capacitor of claim 1, further comprising a second low dielectric insulator layer provided on said high dielectric material and said interdigitized patterns.

5. The decoupling capacitor of claim 1, further comprising a polish stop provided on each of said two interdigitized patterns.

6. The decoupling capacitor of claim 5, wherein said polish stop comprises diamond-like carbon.

7. The decoupling capacitor of claim 5, wherein said polish stop is non-conformally deposited on said interdigitized patterns.

8. The decoupling capacitor of claim 5, wherein said polish stop comprises silicon nitride.

9. The decoupling capacitor of claim 1, wherein said first low dielectric insulator layer comprises fluorinated glass.

10. A capacitor for a semiconductor device, said capacitor comprising:

a first low dielectric layer;

a plurality of interdigitized metal wires provided on said first low dielectric layer;

high dielectric material provided between said plurality of interdigitized metal wires; and

a second low dielectric layer provided on said high dielectric material.

11. The capacitor of claim 10, wherein said high dielectric material comprises tantalum pentoxide.

12. The capacitor of claim 10, wherein said high dielectric material comprises silicon nitride.

13. The capacitor of claim 10, further comprising a polish stop provided on each of the plurality of interdigitized metal wires.

14. The capacitor of claim 13, wherein said polish stop comprises diamond-like carbon.

15. The capacitor of claim 13, wherein said polish stop is non-conformally deposited on said plurality of interdigitized metal wires.

16. The capacitor of claim 13, wherein said polish stop comprises silicon nitride.

17. A method of manufacturing a capacitor, the method comprising:

forming interdigitized metal wires on a first low dielectric material;

depositing a high dielectric material between each of said interdigitized metal wires; and

depositing a second low dielectric material on said high dielectric material such that said interdigitized metal wires are provided between said first and second low dielectric material.

18. The method of claim 17, further comprising depositing polish stop material at least on said metal wires prior to depositing said high dielectric material.

19. The method of claim 17, wherein said polish stop is also deposited on said first low dielectric material between said interdigitized metal wires.

20. The method of claim 19, further comprising etching back said high dielectric material at least to a top surface of said interdigitized metal wires.

21. A method of manufacturing a capacitor, the method comprising:

depositing high dielectric material on a first low dielectric material;

etching a trough region in said high dielectric material;

filling said trough region with metal; and

depositing second low dielectric material on said trough region filled with said metal and said high dielectric material.

22. The method of claim 21, further comprising depositing an etch stop layer on said first low dielectric material such that said etch stop layer is between said high dielectric material and said first low dielectric material.

23. The method of claim 22, further comprising removing said etch stop layer from areas within said trough region after etching said trough and prior to filling said trough region with said metal.

24. A circuit for monitoring a plurality of capacitor segments, the circuit comprising:

a charge monitoring circuit coupled to each capacitor segment;

a coupling circuit for selectively coupling and decoupling one of said capacitor segments from among a plurality of states; and

a control circuit for sequentially controlling said coupling circuit of each of said capacitor segments so as to disconnect a failed capacitor segment while said other capacitor segments are monitored.

25. The circuit of claim 24, wherein each of said capacitor segments comprises a plurality of plates and wherein said coupling circuit comprises at least one n-channel transistor connected between said control circuit and a plate of said capacitor segment.

26. The circuit of claim 25, further comprising a fuse circuit provided between said capacitor segment and said at least one n-channel transistor.

27. The circuit of claim 24, wherein each of said capacitor segments comprises a plurality of plates and wherein said coupling circuit comprises at least one p-channel transistor connected between said control circuit and a plate of said capacitor segment, the other plate of the capacitor segment being connected to a ground potential.

28. The circuit of claim 27, wherein said coupling circuit further comprises a fuse circuit connected between said control circuit and said at least one p-channel transistor.

29. The circuit of claim 24, wherein said charge monitoring circuit outputs a signal based on an amount of current flowing through said capacitor segment when said coupling segment is in a test state.

30. The circuit of claim 24, wherein said charge monitoring circuit comprises an integrator circuit.

31. The circuit of claim 24, wherein the control circuit controls the coupling circuit such that the capacitor segment is disconnected only after failing at least twice.

32. A circuit for monitoring a plurality of capacitor segments, each capacitor segment comprising a first low dielectric insulator layer, a low resistance conductor formed into at least two interdigitized patterns on a surface of said first low dielectric insulator layer and high dielectric material provided between said two interdigitized patterns, the circuit comprising:

a charge monitoring circuit coupled to each of said capacitor segments;

a coupling circuit connected to each of said capacitor segments, said coupling circuit selectively coupling and decoupling each capacitor segment to one of a disabled state, an enabled state and a testing state; and

a control circuit connected to said coupling circuit, said control circuit controlling said coupling circuit so as to place said coupling circuit of a

failed capacitor in the disabled state while monitoring remaining ones of said plurality of capacitor segments.

33. The circuit of claim 32, wherein each of said capacitor segments comprises a plurality of plates and wherein said coupling circuit comprises at least one n-channel transistor connected between said control circuit and a plate of said capacitor segment.

34. The circuit of claim 33, further comprising a fuse circuit provided between said capacitor segment and said at least one n-channel transistor.

35. The circuit of claim 32, wherein each of said capacitor segments comprises a plurality of plates and wherein said coupling circuit comprises at least one p-channel transistor connected between said control circuit and a plate of said capacitor segment, the other plate of said capacitor segment being connected to a ground potential.

36. The circuit of claim 35, wherein the coupling circuit further comprises a fuse circuit connected between said control circuit and said at least one p-channel transistor.

37. The circuit of claim 32, wherein said charge monitoring circuit outputs a signal based on an amount of current flowing through said capacitor segment when said coupling segment is in the testing state.

38. The circuit of claim 32, wherein said charge monitoring circuit comprises an integrator circuit.

39. The circuit of claim 32, wherein the control circuit controls the coupling circuit such that the failed capacitor segment is placed in the disabled state only after failing at least twice in the testing state.